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EXAMINER
WANG, JIN CHENG

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2672	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/091,384	Applicant(s) OBEROI ET AL.	
	Examiner Jin-Cheng Wang	Art Unit 2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/12-27-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 8-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poole et al. U.S. Patent No. 5,798,767 (hereinafter Poole).

Claim 1:

(a) Poole teaches a circuit comprising:

A subtractor coupled to receive a first input and second input (e.g., See the subtractor 160, 180 and 210 of Figure 7; See also Figures 8A-8C, and 3-4);

A multiplier coupled to a third input and an output of the subtractor (e.g., See the multiplier 162, 182, 212 of Figure 7; See also Figures 8A-8C, 3-4);

An adder coupled to a fourth input an output of the multiplier (e.g., See the adder 164, 184 and 214 of Figure 7. See also Figures 8A-8C, and 3-4);

A first multiplexor whose output drives the first input (e.g., See the first multiplexor Tex_g connecting to the subtractor 180 of Figure 7; See also Figures 8A-8C, 3-4);

A second selection whose output drives the second input (e.g., See FogColor_g connecting to the subtractor 180 of Figure 7. Note that FogColor_g is selectable. See also Figures 8A-8C; column 7, lines 5-12; column 7, lines 60-67; column 8, lines 44-50);

A third multiplexor whose output drives the third input (e.g., See the multiplexor Fog_Mult or the multiplexor 194 connecting to the multiplier 162 or 182 of Figure 7. See also Figures 8A-8C);

A fourth multiplexor whose output drives the fourth input (e.g., See the multiplexor 196 connecting to the adder 184 in Figure 7. See also Figures 8A-8C).

(b) However, Poole does not implicitly teaches a second multiplexor whose output drives the second input.

(c) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated multiplexor into the Poole's circuit because such a construction would have provided a means for selection of input values as suggested in Poole (Figures 7-8C, column 7, lines 5-12; column 7, lines 60-67; column 8, lines 44-50) wherein the circuit of Poole can be implemented into two modes, i.e., fog mode and color space conversion mode. Poole's circuit involves a selection of values for the second input, FogColor__c, FogColor__g, FogColor__b, because these fog colors take different values under different mode of operations and therefore a multiplexor should be used for such a selection which provides input to the subtractor.

(d) Such modification would have been required to provide a selection for the input values for the subtractor of the Poole's circuit (Figures 7-8C).

Claim 2:

The claim 2 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of control logic configured to drive selection lines of the first, second, third and fourth multiplexors in response to a value in an operation register.

However, Poole further discloses control signal YUV2RGB, PASS, etc. which control selection lines of the first, second, third and fourth multiplexors (e.g., Figure 7-8c, column 6).

Claim 3:

As per Claim 3, Poole further discloses the first multiplexor passes a color value such as Tex_g to the first input, the second selector passes a color value such as FogColor__g, to the second input, the third multiplexor passes an alpha value such as Fog_Mult, to the third input and the fourth multiplexor passes the color value such as FogColor__g to the fourth input (e.g., Figure 7-8c, column 6-8).

Claims 4-5:

The Claims 4-5 recite similar limitation to that set forth in the Claim 3. The Claims 4-5 are subject to the same rationale of rejection set forth in the Claim 3.

Claim 8:

The claim 8 is subject to the same rationale of rejection set forth in the Claim 1.

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 8 except additional claimed limitation of the color depth precision of the accumulation buffer being larger than the color depth precision of the image buffer.

However, Poole further discloses data cache 106 storing the color values originated from RAM 110 and a write data queue 142 storing the outputs of the processed color values and the

data values can be fed back to the pixel transfer unit. Poole addresses the number of bits in the pixels associated with the image buffer and the accumulation buffer (e.g., Figure 2-4; 7-8c, column 3-9).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 8 except additional claimed limitation of one or more circuit elements configured to transfer the stream of output pixels to a programmable destination.

However, Poole further discloses data cache 106 storing the color values originated from RAM 110 and a write data queue 142 storing the outputs of the processed color values and the data values can be fed back to the pixel transfer unit (e.g., Figure 2-4; 7-8c, column 6).

Claim 11:

The claim 11 encompasses the same scope of invention as that of claim 10 except additional claimed limitation of the programmable destination being the accumulation buffer.

However, Poole further discloses data cache 106 storing the color values originated from RAM 110 and a write data queue 142 storing the outputs of the processed color values and the data values can be fed back to the pixel transfer unit. The Examiner interprets the accumulation buffer as the data storage memory such as the data cache 106 and the write data queue 142 of Poole (e.g., Figure 2-4; 7-8c, column 6).

Claim 12:

The claim 12 encompasses the same scope of invention as that of claim 10 except additional claimed limitation of the programmable destination being the image buffer.

However, Poole further discloses data cache 106 storing the color values originated from RAM 110 and a write data queue 142 storing the outputs of the processed color values and the data values can be fed back to the pixel transfer unit. The Examiner interprets the image buffer as the data storage memory such as the data cache 106 and the write data queue 142 of Poole (e.g., Figure 2-4; 7-8c, column 6).

Claim 13:

The claim 13 encompasses the same scope of invention as that of claim 8 except additional claimed limitation of the programmable operation being one or more of an addition operation, a multiply operation, an accumulate operation, a dynamic blending operation, a matrix-vector multiplication, a load operation and a return operation.

However, Poole further discloses a mixture of such operations (e.g., Figure 2-4; 7-8c, column 6-9).

Claim 14:

The claim 14 encompasses the same scope of invention as that of claim 13 except additional claimed limitation of one or more of the circuit instances being an accumulator register for accumulating sums over multiple of the computational cycles.

However, Poole further discloses data cache 106 storing the color values originated from RAM 110 and a write data queue 142 storing the outputs of the processed color values and the data values can be fed back to the pixel transfer unit. The Examiner interprets the accumulator register as the data storage memory such as the data cache 106 and the write data queue 142 of Poole (e.g., Figure 2-4; 7-8c, column 6-9).

3. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poole et al. U.S. Patent No. 5,798,767 (hereinafter Poole) in view of Buckley et al. U.S. Patent No. 6,104,836 (hereinafter Buckley).

Claim 6:

(a) The Claim 6 encompasses the same scope of invention as that of the claim 1 except additional claim limitation of an input line to the accumulator register coupled to the output of the adder, wherein an output line of the accumulator register couples to an input of the fourth multiplexor.

(b) Poole does not implicitly teaches the claim limitation of an input line to the accumulator register coupled to the output of the adder, wherein an output line of the accumulator register couples to an input of the fourth multiplexor.

(c) However, Buckley teaches the claim limitation of an input line to the accumulator register coupled to the output of the adder, wherein an output line of the accumulator register couples to an input of the fourth multiplexor (Buckley Figure 4; column 4-5).

(d) It would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the path from the accumulator register coupled to the multiplexor of Buckley into the Poole's circuit because such a construction would have provided a fed-back path so that the output of the accumulator can be fed back to the input of the adder.

Moreover, Poole further discloses data cache 106 storing the color values originated from RAM 110 and a write data queue 142 storing the outputs of the processed color values and the

data values can be fed back to the pixel transfer unit (Poole figures 2-4) and therefore Poole suggests a fed back path to the circuit.

(e) Such modification would have been required to provide the circuit architecture to calculate multiple sums at a number of clock cycles (Buckley column 3-5).

Claim 7:

The Claim 7 recites similar limitation to the Claim 6 and 3. The Claim 6 is subject to the same rationale of rejection set forth in the Claims 3 and 6.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6606 for regular communications and (703) 308-6606 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 395-3900.

jcw
March 8, 2004

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600